

Domino in Adiabatic Logic Circuits for Brain Tumor in MRI Signal Processing

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Wide-fan-in OR Gates have large number of leaky parallel transistors connected between dynamic node and Ground and large dynamic node capacitance which increase delay. In this work, a new domino circuit called LECTOR Current Comparison Domino (LCCD) is proposed which has low power consumption and act as a potential drop switching device. The leakage current of LCCD is low in pull up network (PUN) and dynamic node capacitance is greatly reduced by using current mirror technique which can be used in dynamic quasi adiabatic logics. The dynamic node is separated from the PUN using the current comparison stage and the loss in speed due to LECTOR configuration is compensated by increasing mirror ratio and allow the recycling of energy. LECTOR (LEakage Control TransisOR) is introduced in the path between pull-up network and the footer transistor reducing the static leakage current as well as dynamic switching current. LCCD is simulated using 16-nm high performance Predictive Technology Model (PTM) and 15% of power reduction was observed from LCCD for 64 bit OR gate compared with Current Comparison Domino (CCD). This dominoes used in real time adiabatic circuits to realise battery operated applications-portable devices with high speed.

Key words: Pull up network, Dynamic power dissipation, keeper transistor, LECTOR.

Advanced picture preparing empowers the reversible, practically commotion free adjustment of a picture as a grid of whole numbers rather than the traditional darkroom controls or filtration of time-ward voltages important for simple pictures and feature signals. Despite the fact that numerous picture handling calculations are to a great degree influential, the normal client frequently applies operations to computerized pictures without sympathy toward the hidden standards behind these controls. The pictures that

outcome from rushed control are regularly seriously corrupted or overall bargained concerning those that could be delivered if the force and flexibility of the advanced handling programming were effectively used. The increasing speed and complexity of today's designs indicates a significant increase in wide variety of techniques to shrink the power consumption of VLSI chips. In recent year ICs of 100 million transistors were clocked above 1GHz thus power considerations is given more weight comparable to area and speed¹⁶. The different types of currents that contribute to power dissipation are leakage current, standby current, short-circuit current and capacitance current. Leakage current is the current flowing through the parasitic reverse biased diodes formed between the drain bulk and source bulk

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regions¹ and reduction in transistor scaling induces short channel effect¹⁴.

Power dissipation is classified into static power dissipation and dynamic power dissipation. The leakage power and standby power comes under static power dissipation. The short-circuit power dissipated due to short circuit current comes under dynamic power dissipation. High performance in dominos logic can be obtained by dynamic power dissipation². Dynamic power dissipation is given

$$P = ACV^2F \quad \dots(1)$$

Where P is the dynamic power dissipation, A is the activity factor, i.e., the portion of the circuit that is switching, C is the capacitance, V is the supply voltage, and F is the clock frequency of the circuit. Dynamic power dissipation can be reduced by reducing the frequency of operation of the domino circuit, reducing the swing voltage and by reducing the dynamic node capacitance. Reducing frequency of operation reduces speed while reducing voltage swing increases delay.

Analysis of footerless domino logic

The standard footerless domino is one of the important domino logic circuit. Performance and robustness are key factors in designing domino dynamic logic circuits. Keepers are used in standard domino circuit to improve robustness. The use of keepers increases current contention between the keeper transistors and the pull down network. It also increases delay of the circuit. Several approaches are proposed by researchers to overcome this problem. Most of the methods gain one parameter at the expense of losing the other parameter. The circuit techniques devised fall into three categories. They are

- 1) Techniques that tries to modify the circuit that controls the gate voltage of the keeper transistor,
- 2) The circuits that rely on the topology of the footer transistor and
- 3) The circuits that reengineer the evaluation network.

Circuits proposed in the literature like Conditional Keeper Domino⁶ (CKD), High Speed Domino⁷ (HSD), Leakage Current Replica Keeper Domino⁸ (LCR Keeper), and Controlled Keeper by Current Comparison Domino⁹ falls into the first category. Diode Footed Domino⁵ (DFD) falls into the second category. Diode Partitioned Domino (DPD) falls into the third category¹⁰. The Current

Comparison Domino¹ (CCD) and proposed LECTOR Current Comparison Domino (LCCD) falls into both the second and the third categories.

Proposed lector CCD (LCCD)

LECTOR is a technique used for power reduction. Reducing threshold voltage suitable to voltage scaling leads to increased sub-threshold leakage currents and increased power dissipation in CMOS circuits. In LECTOR a p-type transistor is connected in series with an n-type transistor with the gate terminals of both transistors connected to the source terminals of each other transistor. One transistor in this configuration always operates near cut-off region increasing the resistance between VDD and GND thus reducing leakage current¹⁷. Current Comparison based Domino is a technique which improves robustness, noise immunity¹ by comparing the pull up network current with the worst case leakage current. The keeper transistor is switched off when unnecessary to reduce contention. Switching off the keeper transistor results in reduces power. The proposed circuit LECTOR CCD shown in Fig 5 is obtained by adding LECTOR shown in Fig 3 in a suitable branch of the Current Comparison Domino circuit shown in Fig 4.

The LECTOR transistor is connected in series in the branch containing nodes N1 and N2 as shown in the Fig 5. Power dissipation increases with decrease in resistance between VDD and GND. In the LECTOR transistor configuration the potential difference between the node N1 and N2 is high when the pull up network is OFF. When the pull up network is ON the potential at node N1 tries to come down to reach the ground potential, switching off the NMOS LECTOR transistor.

The functioning of LECTOR prevents N1 from reaching the ground potential thus the resistance of LECTOR configuration increases. The resistance of the LECTOR MOSFET in linear region is given by

$$R = K \left(\frac{L}{W} \right) \quad \dots(2)$$

With

$$K = \frac{1}{\mu C_{ox}(V_{gs} - V_t)} \quad \dots(3)$$

Where L and W are given by Length and Width of transistor respectively, V_{gs} and V_t are gate

to source voltage and threshold voltage, λ the channel-length modulation parameter which models current dependence on drain voltage due to the Early effect, or channel length modulation and K is technology dependent parameter. The above discussed LECTOR configuration is added between the pull up network and the bottom footer transistor.

Circuit operation

The circuit operates in two phases namely 1) Pre-discharge phase and 2) Evaluation Phase

1) Pre-discharge phase: In pre-discharge phase the clock signal is low and all inputs to pull up evaluation network are high. The M_{pre} transistor conducts and hence node A is at potential VDD. M_1 and M_2 transistors are switched off. The M_{Dis}

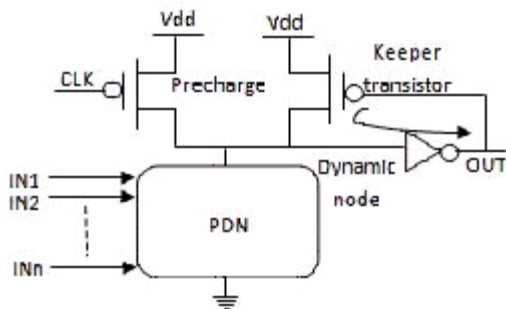


Fig. 1. Standard Footerless Domino (SFLD)⁵

transistor is ON and discharges the dynamic node to 0 volts. The current reference circuit is switched off during the pre discharge phase by the internal circuitry. Transistor M_{Eval} is off.

2) Evaluation phase: During the evaluation phase the clock signal is high and the inputs to pull up evaluation network may be high or low. In this phase the LECTOR transistor configuration significantly contributes to power reduction. There are two cases. All inputs may be high and the pull up evaluation network is off or at least on input may be low switching on the pull up evaluation network. In the first case leakage current flows through the pull up evaluation network. This leakage current is less compared with Current Comparison Domino because of the LECTOR transistor in series with the pull up evaluation network in the LCCD. The reference circuit does not contain LECTOR transistor for area minimization purposes and hence generates a larger compensating current. If the leakage current is mirrored as such by transistor M_2 there is a possibility that dynamic node may be susceptible to noise. To overcome this problem transistor M_2 is upsized.

In the second case the current in the pull up evaluation network tries to go up but the LECTOR transistor limits the current. This results in reduced gate voltage of transistor M_2 . But since

Table 1. Sizing of Transistors in LCCD

Fan-In	Width of Transistors								
	M1	M2	M3	M4	MPre	MEval	MDis	Mk	Inverter (PMOS/NMOS)
8 Inputs	$7L_{min}$	$16L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$14L_{min} / 7L_{min}$
16 Inputs	$7L_{min}$	$16L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$14L_{min} / 7L_{min}$
32 Inputs	$7L_{min}$	$16L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$14L_{min} / 7L_{min}$
64 Inputs	$7L_{min}$	$16L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$7L_{min}$	$14L_{min} / 7L_{min}$

Table 2. Implemented functions of logic unit

Domino logic function	Arithmetic operation
OR	Increment
AND	Subtractor
NOR	Multiplier
NAND	Decrement

it is upsized for the same voltage M_2 generates the higher current resulting in negligible speed degradation in charging and discharging of the capacitance in the dynamic node.

Transistor sizing

LECTOR configuration (Fig 3) increases the resistance between the power rails reducing power dissipation. Reduced current due to increased resistance by LECTOR takes more time

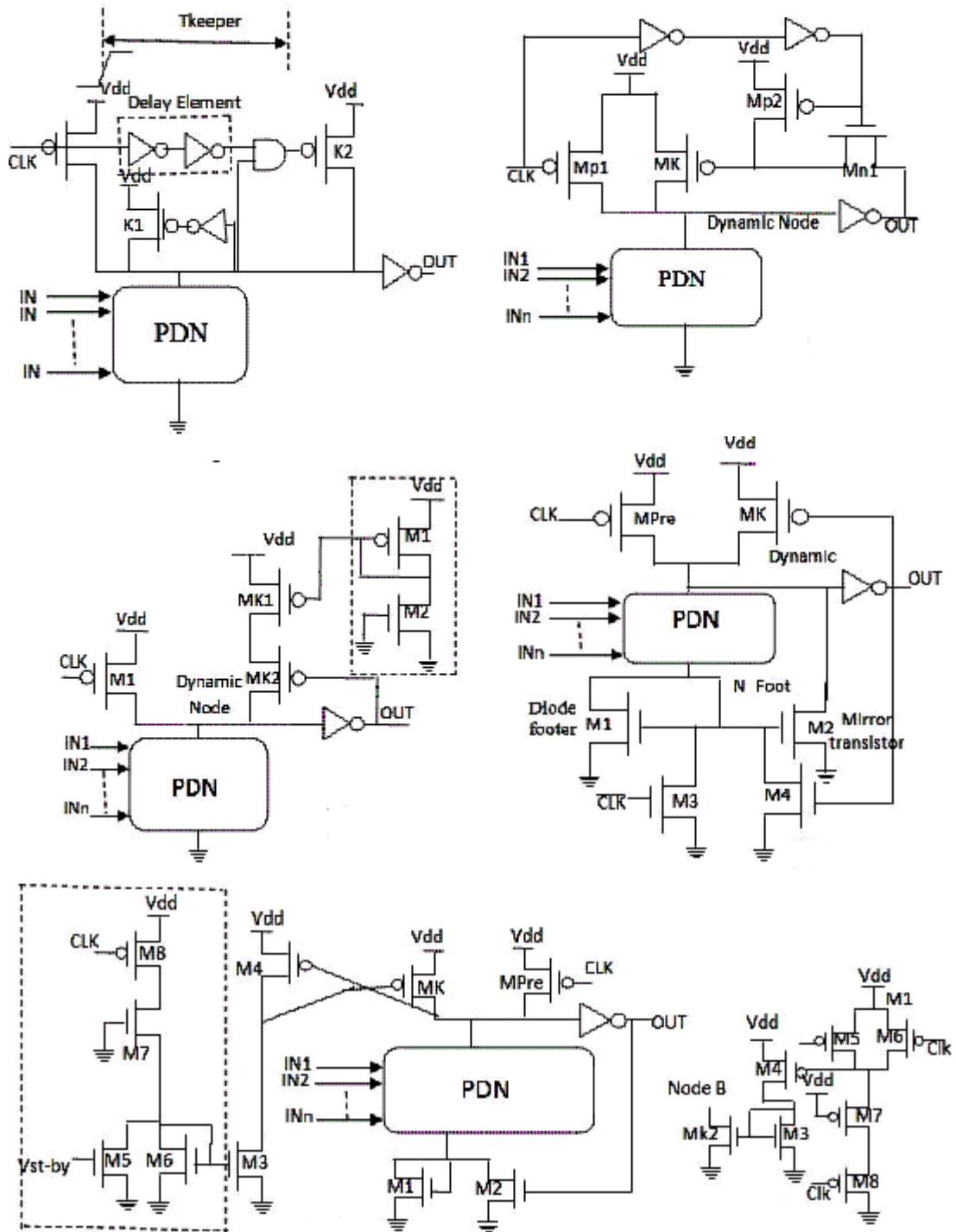


Fig. 2. (a) CKD⁶ (b) HSD⁷ (c) LCR Keeper⁸ (d) DFD⁵ (e) CKCCD⁹ (f) I.Ref circuit

to charge the dynamic node capacitance to a fixed voltage and lead to increased charging and discharging time in LCCD (Fig 5). To overcome this problem transistor M2 is to be upsized. Upsized transistor M2 produces more current in saturation for the same gate voltage. The problem of delay is thus avoided and the mirror ratio is of the transistor M2 when compared with the transistor M1 is given by

$$M = \frac{(W/L)M2}{(W/L)M1} \dots(4)$$

where W and L is given by width and length of the transistor. The PMOS transistor operates slowly compared to the NMOS counterpart because the mobility of holes is half that of the electrons. The output inverter has to be

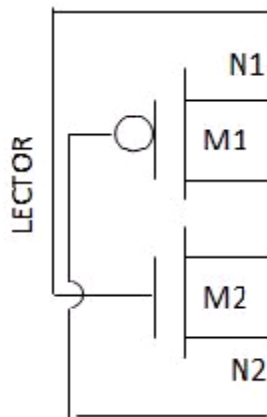


Fig. 3. LECTOR Configuration

a skew less inverter. If the inverter is skewed the output either falls quickly or rises quickly. To make the output inverter skew less the width of the PMOS transistor is made twice compared to the NMOS transistor. The L_{min} is chosen as 16nm and the width of the upsized M2 transistor is chosen to be $16L_{min}$. All the values of transistor sizing in LCCD is shown in table 1.

Simulation & Results

The circuit is simulated using 16nm High Performance Predictive Technology model with T-Spice. Clock speed used for simulation is 1 GHz. Nominal supply voltage of $V_{DD} = 0.8V$ and temperature of $110^{\circ}C$ is used for simulation. Only one of the inputs to pull up evaluation network is allowed to change during the evaluation phase. The length of all transistors is assumed to be equal to the minimum length L_{min} which is 16nm. The width of PMOS transistor in output inverter is twice with respect to the NMOS counterpart [1]. The schematic Layout and instantaneous power, output waveforms and line chart between various techniques Vs Normalized Power are shown in Fig.6 (a) , Fig.6 (b) & Fig 6 (c) respectively. Leakage current consumption in LCCD is reduced by the LECTOR network. Either the NMOS or PMOS transistor in LECTOR will be Near Cut-OFF state at all the time or in ON state i.e., saturation state very occasionally [17]. The major part of leakage current is the sub threshold current, which is given by

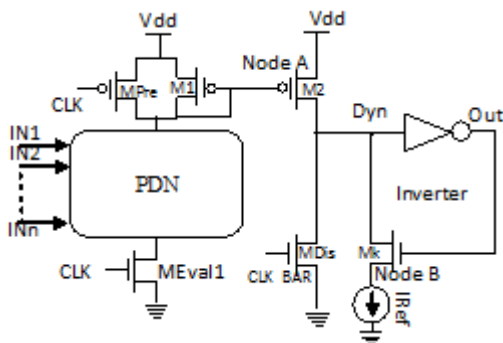


Fig. 4. Current Comparison Domino (CCD)

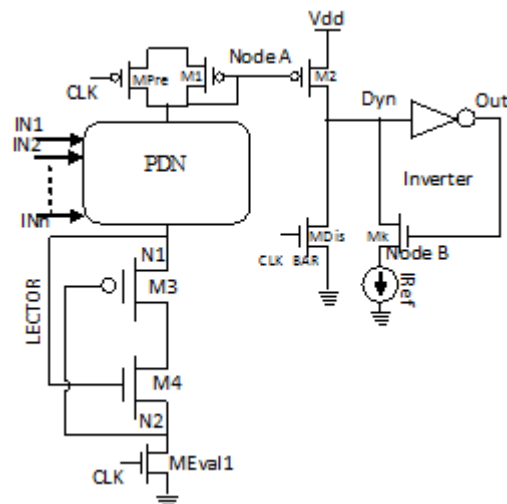


Fig. 5. LECTOR Current Comparison Domino

$$I_{sub_th} = I_o(1 - e^{-\frac{V_{ds}}{V_t}}) e^{\frac{(V_{gs} - V_{th} - \eta V_{ds})}{nV_t}} \dots(5)$$

with

$$I_o = \mu_o C_{ox} W / L(n-1)V_t^2 \dots(6)$$

where V_{gs} is gate to source voltage of the transistor, V_{ds} is drain to source voltage of the transistor, η is the DIBL coefficient, C_{ox} is the gate oxide capacitance, $V_t = KT/q$ is the thermal voltage, n is the sub threshold swing coefficient, μ_o is the zero bias mobility and L and w are the length and width of the transistor. Reduction in leakage current is obtained by reducing sub threshold leakage current by increasing the resistance between PDN and ground node using LECTOR. Thus 15%,13%,12.5% and 11.5% of power reduction is obtain when compared with 64 bit,32 bit,16 bit and 8 bit CCD OR gate respectively and results are tabulated in table 2.

Application of dominos using parallel

Nowadays CMOS technology variation process faced a new challenges in designing roubust circuits. In adiabatic circuits if mainly concentrate on energy consumptions and process variation in the losses. These domino circuits provide low power consumption and occupy less space with high operationg speed.These domino circuits can be used to design various inner part for asymptotically and for static and dynamic quasi adiabatic logic with low power. The circuit techniques devised fall into three categories. They are

1. Techniques that tries to modify the circuit that controls the gate voltage of the keeper transistor
2. The circuits that rely on the topology of the footer transistor and
3. The circuits that reengineer the evaluation network.

In domino circuits dynamic power dissipation can be reduced by reducing the frequency of operation of the domino circuit, reducing the swing voltage and by reducing the dynamic node capacitance. Reducing frequency of operation reduces speed while reducing voltage swing increases delay due to large dynamic node capacitance and wide-fan-in domino OR gates have large number of leaky parallel transistors connected between dynamic node and ground. Domino is the better design strategy used to minimize power

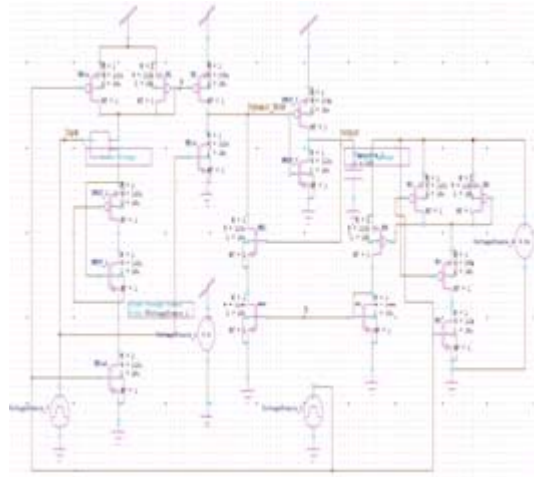


Fig. 6(a). Schematic Layout of 8 input OR Gate

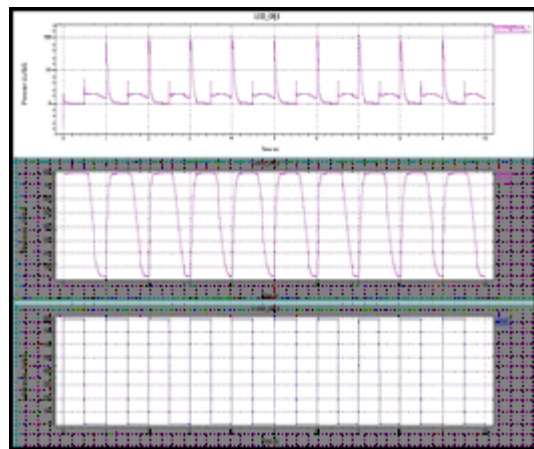


Fig. 6(b). Instantaneous Power & Output Waveforms

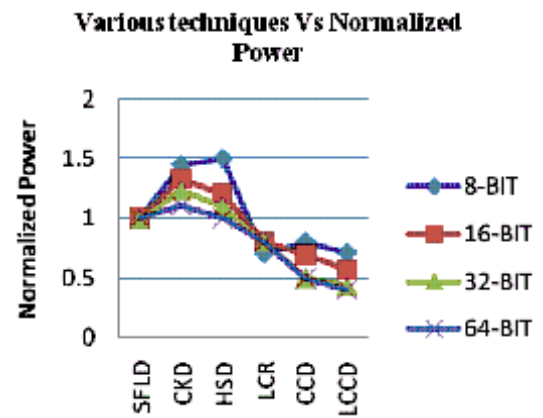


Fig. 6(c). Various techniques Vs Normalized power

consumption and to make better trade-off between power, delay and area.

Brain tumor of both mass and malignant tumor in MRI images are segmented using K-Means algorithm, Fuzzy C Means algorithm, Gray Level Cooccurrence matrix features, combination of both Gray Level Cooccurrence matrix features

Output achieved using domino circuits for brain tumor in MRI signal processing :

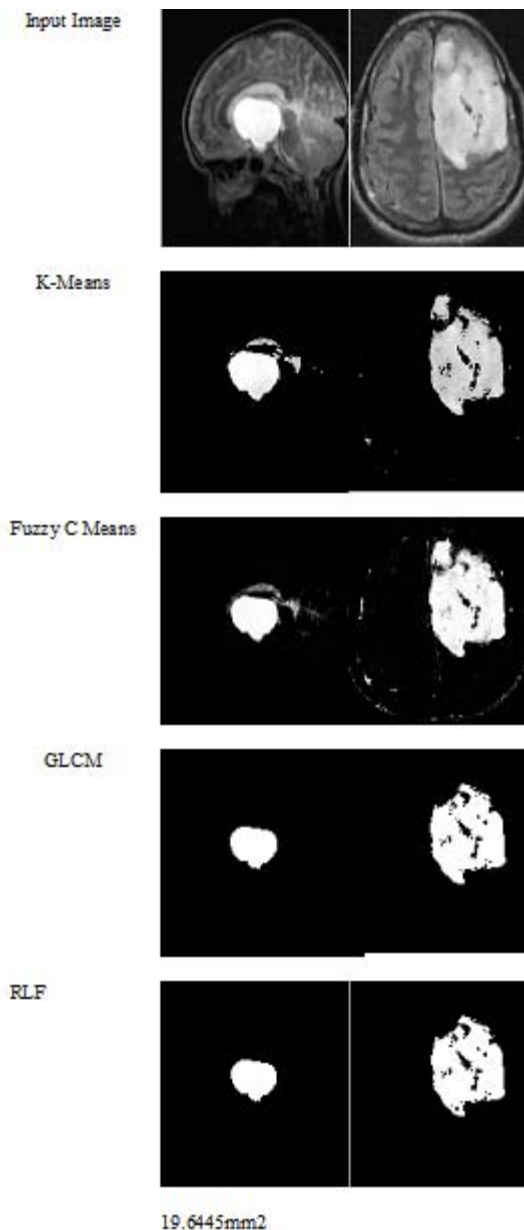


Fig. 7. MRI signals achieved using domino circuits

and Gray Level Run Length matrix features of texture based segmentation achieved using domino circuits for brain tumor in MRI signal processing .

CONCLUSION

High performance and robustness in wide fan in dynamic gates are obtained by transistor scaling in dimension, choosing threshold voltage and supply voltage which increases leakage power dissipation. The motivation for the proposed design is obtained from contest going between power consumption, delay and area. A new technique is proposed by adding LECTOR between PDN and ground and we call this technique as LCCD. Unlike other leakage control technique, the NMOS and PMOS which is used in LECTOR will not need any controlling input to monitor the state of the transistor. By this advantage it increases the resistance between PDN and ground which reduces leakage power consumption .Our experimental result gives 15%, 13%, 12.5% and 11.5% of power reduction compared with 64 bit, 32 bit, 16 bit and 8 bit wide fan in CCD domino OR gate with PTM V2.1 of 16nm technology at a power supply of 0.8V. Thus the proposed LCCD wide fan in domino OR gate is very effective in power reduction and also thus the low-leakage dominos reducing the thresholding and can be used for battery operated portable adiabatic logic circuits.

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